Amendments to the Specification

Please substitute the paragraph following heading "CROSS-REFERENCE TO RELATED APPLICATIONS" with the following paragraph:

This application is a continuation of U.S. Patent Application No. 10/163,871, filed June 7, 2002, entitled "Receiver Having Decisional Feedback Equalizer With Remodulation and Related Methods," which claims priority to U.S. Provisional Patent Application No. 60/296,457, filed June 8, 2001, entitled "Generalized DFE Architecture with Remodulation," the contents of each is hereby incorporated by reference in its entirety.

Please amend the following paragraphs/sections as follows.

- Please amend paragraph 20 as follows:

A carrier loop portion 154 estimates the frequency offset, that is, generates a frequency-offset estimate ω representative of the undesired frequency offset, based at least in part on decision signal 142. Carrier loop portion 154 generates correction signal 122 such that it has a frequency equal to frequency-offset estimate ω. For example, carrier loop portion 154 may generate correction signal 122 as a series of samples of a complex sinusoidal signal represented by the term $e^{-j\omega n}$, where n is a time index indicating the n^{th} sample of signal 122. Alternatively, signal 122 may be a continuous-time signal represented by the term $e^{-j\omega t}$, where t represents time.

- Please amend paragraph 28 as follows:

In receiver 200, the order of multiplier 120 and combiner 126 is reversed with respect to the order in receiver 100. That is, combiner 126 precedes multiplier 120. In receiver 200, combiner 126 combines filtered signal 112 with restorative signal 212 to produce an intermediate signal ~~230~~ 231 substantially free of ISI, but having the frequency offset present in input signal 102. Multiplier 120 frequency-shifts intermediate signal ~~230~~ 231 toward baseband responsive to frequency-offset estimate ω, and more specifically, responsive to frequency correction signal 122, thereby producing a baseband signal 232. Baseband signal 232 is substantially free of both the frequency offset and the ISI.

- Please amend paragraph 34 as follows:

In receiver 200, combiner 126 combines filtered signal 112 with restorative signal 212 to produce intermediate signal ~~230~~ 231 substantially free of ISI. That is, combiner 126 combines spectrum B (in column 304) having notch 308 with spectrum C (in column 304) including frequency-correction spectrum 310 to produce spectrum D (in column 304). Spectrum D (in column 304) thus represents the sum of spectrums B and C. In column 304, since frequency-correction spectrum 310 and notch 308 coincide-in-frequency with each other, spectrum D has a substantially flat passband and an excellent Signal-to-Noise ~~ration~~ ratio (SNR). In the time domain, the effect of the flat spectral passband is a substantially reduced or eliminated ISI in signals ~~230~~ 231 and 232 of receiver 200. In column 304, the flat spectral passband of spectrum D illustrates a near perfect match between filter 106 and DFE 150 as used in restorative signal generator 210. In contrast, in receiver 100, signal 124

has corrupted spectrum D (in column 302) that causes a significantly degraded SNR and substantial ISI.

- Please amend paragraph 35 as follows:

In receiver 200, multiplier 120 frequency-shifts intermediate signal ~~230~~ 231 to baseband responsive to frequency correctional signal 122, thereby producing baseband signal 232 substantially free of ISI and the undesired frequency offset. Signal 232 has spectrum E in column 304. Spectrum E in column 304 has a substantially flat passband, equating to minimal ISI. In contrast, in receiver 100, signal 132 has corrupted spectrum E in column 302.

- Please amend paragraph 38 as follows:

FIG. 5 is a block diagram expanding on portions of restorative signal generator 404 of receiver 400. Depicted in FIG. 5, are multipliers 226 and 408, and a detailed block diagram of DFE 150. DFE 150 includes a delay stage 502 including cascaded delay ~~unit~~ units 502a-502c, coupled to a weighting stage 506 including multipliers 506a-506c associated with respective weights C_0 - C_2, and a combiner 510. The coefficients are also used for filtering in filter 106.

- Please amend paragraph 39 as follows:

Delay stage 502 produces successive time-delayed portions 512a, 512b and 512c of frequency-shifted decision signal 230. For example, in an arrangement where signal 230 includes signal samples, time-delayed portions 512 are time-delayed samples of signal 230.

Weighting stage 506 weights time-delayed portions 512a, 512b and 512c with respective coefficients C_0, C_1 and C_2, to produce weighted, time-delayed portions 516a, 516b and 516c. Combiner 510 combines weighted portions 516 to produce signal 212. Delay stage ~~702~~ 502 and weighting stage 506 may include more or less unit delays and weighting units (that is, multipliers), respectively.

- Please amend paragraph 48 as follows:

FIG. 9 is a flow chart of an example method 900 of processing a received signal that can be implemented in a receiver, such as receiver 200, 400, or 600 for example. It is assumed the receiver receives a received signal (for example, signal 102) including symbols and a frequency offset from baseband. It is also assumed the receiver generates an estimate of the frequency offset (for example, frequency-offset estimate ω), by way of a receiver carrier loop, for example.

- Please amend paragraph 58 as follows:

Exemplary arrangements of receivers 100, 200, 400 and 600 may operate on complex signals, which may be continuous-time or sampled signals. That is, some or all of the signals discussed above, such as signals 102, 108, 112, 122, 212, and so on, may be complex signals. In such arrangements, the components of the receivers perform complex operations. For example, multipliers 120, 226, ~~506~~ 408 and ~~707~~ 704 perform complex multiplication operations. Other arrangements are possible, for example, wherein the receivers operate on non-complex continuous-time or discrete-time signals.